UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,866	03/26/2004	Kazuo Hotaka	2905-108	7608

6449 7590 06/19/2006

ROTHWELL, FIGG, ERNST & MANBECK, P.C.
1425 K STREET, N.W.
SUITE 800
WASHINGTON, DC 20005

EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,866	HOTAKA, KAZUO	
	Examiner	Art Unit	
	Daniel Kim	2185	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received March 26, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Information Disclosure Statement(s) is being considered by the examiner.

Where the provided translation of a foreign patent publication was limited to the abstract, only the abstract has been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 and 13 are rejected under under 35 U.S.C. 102(b) as being anticipated by Leon et al (US Patent No. 6,119,210).

For claim 1, Leon discloses a circuit for prevention of unintentional writing to a memory, comprising:

a detection circuit that detects a drop in power supply voltage and outputs a first reset signal in response thereto, said detection circuit being capable of being turned on and off by a control signal from a control terminal (supply voltage drop detection circuits prohibit programming, namely the modification of stored data, if the supply voltage of

the memory or of the circuit comprising the memory is below a certain value, col. 1, lines 22-26; a comparator to reset the flip-flop circuit, col. 3, lines 21-22); and

a control signal detecting circuit that detects a change in said control signal and outputs a second reset signal in response thereto (the comparator produces a logic signal whose state is a function of the result of the comparison, this signal being given to the resetting input of the flip-flop circuit, col. 5, lines 5-7);

wherein a data input or output operation to said memory is prohibited in response to either said first reset signal or said second reset signal (programming is permitted when an enabling signal is in a first state and prohibited when this signal is in a second state, the protection means including a supply voltage drop detection device to set the enabling signal in the second state when the supply voltage is below a threshold, col. 3, lines 7-12).

For claim 2, Leon discloses said memory is a nonvolatile memory which requires a voltage above a certain level at the time of writing (the device may be implemented in a non-volatile memory or a circuit comprising such a memory, col. 3, lines 47-48).

For claim 3, Leon discloses a register which registers and outputs the control signal (an internal control register whose contents represent authorization of programming or prohibition of programming, col. 1, lines 30-32),

wherein said register turns on said detection circuit upon a drop in power supply voltage when said register is in a first state (the protection means including a supply voltage drop detection device to set the enabling signal in a state when the supply voltage is below a threshold, col. 3, lines 9-11), and

wherein a data input or output operation to said memory is prohibited by said control signal detecting circuit upon a drop in power supply voltage when said register is in a second state (a device for protection of stored data comprising protection means to control a signal to prohibit programming when a signal is in a second state, col. 3, lines 5-9).

Claim 13 is rejected using the same rationale as for the rejection of claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leon et al (US Patent No. 6,119,210) and Fujimori (US Patent No. 6,788,567).

For claim 4, Leon discloses the invention as per rejection of claim 3 above.

Leon fails to disclose the limitations of the current claim.

Fujimori, however, helps disclose a first inverter connected between said register and said detection circuit and a second inverter to which said control signal of said register is to be inputted, said second inverter being part of said control signal detecting circuit, wherein said first inverter and said second inverter have different threshold levels for determining ON/OFF states thereof (a data holding circuit in which data are held by connecting first and second inverter circuits in a loop at the time of latching

data, col. 2, lines 37-40; the data holding circuit having a loop switching gate interposed between the input node of a first inverter circuit and one end of a nonvolatile memory element, and an output node of a second inverter circuit, and is on at the time of latching and writing data, and off in applying a reading signal, col. 2, lines 53-60). Leon and Fujimori are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include inverters and threshold levels because this would allow for data to be held correctly (col. 3, lines 40-41), as taught by Fujimori.

6. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leon et al (US Patent No. 6,119,210), Fujimori (US Patent No. 6,788,567) and Hongo et al (US PGPub No. 20020129195).

For claim 5, the combined teachings of Leon and Fujimori disclose the invention as per rejection of claim 4 above.

These teachings fail to disclose the limitations of the current claim.

Hongo, however, helps disclose a mode control register that controls operating status of said memory, said mode control register being resettable by either said first reset signal or said second reset signal (reset signals reset a control-signal register, par. 013).

Leon, Fujimori and Hongo are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been

obvious to a person of ordinary skill in the art at the time of the invention to include a resettable mode control register because this would allow for rewriting and discontinuing rewriting operations (par. 0138), as taught by Hongo.

For claim 14, the combined teachings of Leon, Fujimori and Hongo disclose the invention as per rejections of claims 5 and 13 above.

Hongo further helps disclose a microcomputer wherein said microcomputer, said detection circuit, said control signal detecting circuit and said memory are integrally formed as a single chip on a semiconductor substrate (a microcomputer in which a programmable nonvolatile memory is built, par. 0002).

7. Claims 6-12 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leon et al (US Patent No. 6,119,210), Fujimori (US Patent No. 6,788,567), Hongo et al (US PGPub No. 20020129195) and Kwon et al (US Patent No. 6,556,504).

For claim 6, the combined teachings of Leon, Fujimori and Hongo disclose the invention as per rejection of claim 5 above.

These teachings fail to disclose the limitations of the current claim.

Kwon, however, helps disclose a read/write controller that outputs a read-enable signal, a write-enable signal and an address signal and also performs inputting/outputting of data to said memory based on an output signal of said mode control register (a read enable signal as a data output signal, col. 6, lines 59-60; a write

enable signal as a data input signal, col. 1, lines 31-32; an address input control signal, col. 7, lines 41-42).

Leon, Fujimori, Hongo and Kwon are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include these signals because they would help control data input/output of different operations in a nonvolatile semiconductor memory device (col. 3, lines 42-44), as taught by Kwon.

Claim 7 is rejected using the same rationale as for the rejections of claims 2 and 6 above.

For claim 8, the combined teachings of Leon, Fujimori, Hongo and Kwon disclose the invention as per rejection of claims 3 and 6 above.

Kwon further helps disclose a standby control signal (the memory device may enter a standby state from a busy state, col. 13, lines 31-32).

Claim 9 is rejected using the same rationale as for the rejections of claims 2 and 8 above.

Claim 10 is rejected using the same rationale as for the rejections of claims 4 and 8 above.

Claim 11 is rejected using the same rationale as for the rejections of claims 6 and 8 above.

Claim 12 is rejected using the same rationale as for the rejections of claims 8-11 above.

Claim 15 is rejected using the same rationale as for the rejections of claims 8 and 12 above.

Claim 16 is rejected using the same rationale as for the rejections of claims 7 and 15 above.

Claim 17 is rejected using the same rationale as for the rejection of claim 8 above.

Claim 18 is rejected using the same rationale as for the rejections of claims 8 and 11 above.

Claim 19 is rejected using the same rationale as for the rejection of claims 15 and 16 above.

Claim 20 is rejected using the same rationale as for the rejections of claims 8, 15 and 18 above.

Citation of Pertinent Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kuwano (US PGPub No. 20020103958) discloses a programmable nonvolatile memory using a register as a source of generating control signals such as write, read, and reset signals.

Kamp et al (US Patent No. 6,201,731) discloses a read-out memory system and logic circuit, and whenever a low power condition is detected, activating a disturb prevent circuit to prevent unintended voltages from disturbing memory.

Contact Information

7. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

6-8-06

PIERRE VITAL
PRIMARY EXAMINER